(Atomistic) Challenges in Predictive Process Simulation

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(Figure from Asen Asenov’s lecture, ChiPPS’2000)
SUBJECTS

• Technologies:
  Mainstream technology is CMOS
  Other (III-V, SiC...) not covered here

• Main issues:
  Dopant profile
  Life time of transistors
  Gate oxide material
  CONTEXT: Miniaturization and power consumption
AGENDA

- Introduction to CMOS
  MOS transistor and its key parameters
  CMOS technology
  The Roadmap: how CMOS will evolve

- Atoms in front-end process simulation
  Granular distribution of charges
  Mechanism of dopant segregation (FHImd example)

- Atoms in reliability simulation
  Gate leakage and predictions of MOS life time
  Mechanism of SiO₂ breakdown (FHImd example)

- Atoms in new materials for CMOS
  High-K dielectrics for gate oxides
  TMO/Si(001) and REO/Si(001) interfaces (FHImd example)

- Summary and conclusions
MOS TRANSISTOR: WORKING PRINCIPLE

Off

Linear

Saturation

source

gate

drain

channel

gate oxide

mos-principle.ps
MOS TRANSISTOR: 130 nm node

Each technology generation has the same relative dimensions.
CMOS (COMPLEMENTARY MOS) PROCESS

Si crystals are grown and cut into wafers

FRONT END: make the device
- implantation; gate stack formation (oxide + polySi)
- Process simulation: implantation & diffusion
- Reliability: gate oxide degradation
- Materials: deposition and properties of dielectrics

BACK END: connect devices into circuits/chips
- silicidation; IL dielectric and metal deposition
- Reliability: electromigration in stressed polymetal

Break into separate chips, add pins, seal, sell
CMOS MATERIALS

• **Substrate**
  Silicon, because it’s cheap and it works
  Si(001), because they know how to handle it

• **Front end (active device)**
  Donors: P, As, maybe Sb
  Acceptors: B, maybe In
  Gate oxide: SiO$_2$ (nitridized), soon high-K (unspecified)
  Gate: poly-Si, maybe poly-SiGe, metal stack for high-K

• **Back end (interconnects)**
  Contacts: TiSi$_2$, CoSi$_2$, WSi$_2$ (gate)
  Interconnects: Al:Cu, Cu
  Interlevel insulator: SiO$_2$ doped with F, H, or/and C
  Diffusion barriers / etch stops: TiN, WN

• **Thermal budget**
  Materials and structures must survive high temperatures:
  Front-end processing: some seconds around 1000°C (RTA)
  Back-end processing: stays below 600°C
SPEEDING ON THE ROAD

ITRS Roadmap Acceleration Continues...
(Including MPU/ASIC "Physical Gate Length" Proposal)

* Note: MPU ASIC Physical Bottom Gate Length Preliminary 2000 Update still under discussion

MPU/ASIC Gate "Physical"

MPU/ASIC Gate "In Resist"

[9/15 - Litho Proposed "In Resist" (70% of "Best Case" Half Pitch)]

[9/15 - Litho Proposed "Physical" (1 year ahead of "In Resist")]

Technology Node - DRAM Half-Pitch (nm)

Year of Production

2001 Renewal Period

REV 1kg_g - 10/20/00

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CONSEQUENCES OF MINIATURIZATION

- Dopant activation: concentrations above solubility
  How to achieve maximum concentration?
  NEEDED: understanding of the activation process

- Dopant profile formation: short annealing times
  How to simulate nonequilibrium processes?
  NEEDED: Atomistic reaction paths

- Statistics of dopant distribution: few dopants in channel
  How to compute statistical variations of transistor parameters?
  NEEDED: Interaction of dopants on atomistic level

- SiO₂ gate dielectric: few atomic layers only
  Does high leakage current kill the oxide?
  NEEDED: Mechanism of oxide breakdown

- SiO₂ gate dielectric: t_{ox} cannot be reduced below ~2nm
  Suitable replacement needed (TM or RE oxide)
  NEEDED: General understanding of high-K dielectrics
PROCESS SIMULATION: DOPING PROFILES

• Old thinking: continuous distribution of charges
  Detailed atomistic mechanisms needed occasionally
  Good if dimensions are larger than about 100 nm

• New thinking: granular distribution of charges
  Detailed atomistic mechanisms will be needed
  Necessary if dimensions smaller than about 50 nm

• Agenda
  Effects of granularity on transistor parameters [1]
  Mechanism of dopant segregation [2]

• 50nm × 50nm transistors: “identical” devices are very different

A. Asenov, in “Challenges in Predictive Process Simulation”, Springer (to be published)
HOW ATOMS CHANGE THRESHOLD VOLTAGE

50 nm x 50 nm transistors, 170 dopant atoms

\[ V_{th} = 0.56 \text{ V} \]
\[ V_{th} = 0.78 \text{ V} \]

A. Asenov, in “Challenges in Predictive Process Simulation”, Springer (to be published)
SEGREGATION: DOPANT STATISTICS UNDER OXIDE

- Source
- Gate
- Drain
- Inversion channel
- Gate oxide
HOW AND WHY DOPANTS SEGREGATE?

Substitution at DB sites
\(~10^{12}\) cm\(^{-2}\) traps available

Pairing of donors
Efficient above \(C_p \sim 10^{19}\) cm\(^{-3}\)

\[\log(D_P), \text{ cm}^{-2}\]

THE DOMINANT MECHANISM

• Most of the segregation is due to imperfect oxidation

\[
\begin{align*}
\text{Si} & \quad \text{O} \quad \text{Si} & \quad \text{O} \\
\text{Si} & \quad \text{P} & \rightarrow & \quad \text{Si} & \quad \text{P} & \quad \bullet & \quad \text{Si} & \quad \text{O} \\
\text{Si} & \quad \text{Si} & \quad \text{Si} & \quad \text{Si} & \quad \text{Si}
\end{align*}
\]

\[
\begin{align*}
\text{O} & \quad \text{O} \quad \text{O} \quad \text{O} \\
\text{O} & \quad \text{Si} & \bullet & \quad \text{Si} & \quad \text{O} & \rightarrow & \quad \text{O} & \quad \text{Si} & \quad \text{Si} & \quad \text{O} \\
\text{Si} & \quad \text{Si} & \quad \text{Si} & \quad \text{Si}
\end{align*}
\]

• Now we have:
  Atomic-scale description of the segregation process
  Boundary conditions for simulation of dopant distribution

• Valid for all concentrations of donor atoms
DIFFUSION OF DANGLING BONDS

P atom in step ledge
-0.1 eV

Initial DB configuration
0.0 eV

Barrier to Si trimer
0.6 eV

Final configuration (Si trimer)
0.3 eV
DOSE LOSS AND P CONCENTRATION

$E_p = 0.63$ eV (0.5±0.3 eV), $N_p = N_o$

$E_t = 0.71$ eV (0.5±0.3 eV), $N_t = 0.18 N_o$
**DOPANT PROFILES: SUMMARY**

- **“Decanano” regime:**
  Charge granularity counts
  Atomistic simulators exist [1]
  Microscopic data incomplete

- **Example 1: MOSFET parameter fluctuations, 50nm x 50nm device**
  Drain current fluctuations reach 200%
  Threshold voltage fluctuations reach 10%
  Consequences: Non-uniform leakage, local failures, power loss

- **Example 2: Dopant segregation to SiO₂/Si(001) interfaces**
  Most of segregation due to imperfect oxidation
  Surface steps are natural segregation sites
  Consequence: Dopant distribution affected by local roughness
  Remark: Dangling bonds are quite mobile in SiO₂

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RELIABILITY: HOW LONG CAN AN OXIDE WORK?

• Leakage changes exponentially with $t_{ox}$
  Supply voltage cannot be too low
  Electrons create damage in SiO$_2$
  Is this a problem or not?

• Reliability predictions
  In 10 years, only 100 parts in a million may fail
  Life time cannot be measured under MOFSET working conditions!
  Measurement: test oxides are electrically overstressed
  Extrapolations over orders of magnitude must be done
  Breakdown models needed, the existing ones are uncertain

• Example:
  Contemporary predictions of reliability
  SILC concept
  Breakdown mechanism
  Which defects may be responsible? (FHImd, [1])

J. Dąbrowski, P. Gaworzewski, T. Guminskaya, A. Huber, in preparation
RELIABILITY OF GATE DIELECTRICS

State-of-the-art SiO₂ gate oxides may fail too early...

STRESS INDUCED LEAKAGE CURRENT

J. Dąbrowski, P. Gaworzewski, T. Guminskaya, A. Huber, in preparation
MECHANISM OF OXIDE BREAKDOWN

Activation of “killer” centers by Anode Hole Injection

Damage extension and TAT center creation
CAN DAMAGE PROCEED IN THIS WAY?

**Step 0:** SiH bond, neutral

**Step 1:** released H builds OH, DB$^+$

**Step 1***: as 1, but DB neutral

**Step 2:** released O builds O-O
RELIABILITY: SUMMARY

• Gate leakage increases exponentially with decreasing $t_{ox}$
  New CMOS generations may suffer from reliability problems [1]

• Reliability is difficult to predict
  Physical models of dielectric breakdown are needed [2]

• Example: Microscopic sequence of breakdown process [3]
  SILC measurements and FHImd calculations
  Hydrogen + current + high electric field = mixing of Si and SiO$_2$:
  1. AHI activates hydrogen to Si-H$^+$
  2. tunneling electron + Si-H$^+$ = Si-OH + Si$_{DB}$(TAT)
  3. AHI activates OH to Si-OH$^+$
  4. tunneling electron + SiSi-OH$^+$ = Si-H + O-O
  5. Si$_{DB}$ recombine, forming Si-Si paths for current (or TAT)
  6. O$^-$ diffuses into the anode and oxidizes the substrate
  CONCLUSION: Reduce Si$_{DB}$/O$^-$ mobility = increase oxide lifetime

NEW MATERIAL: ALTERNATIVE GATE DIELECTRIC

- SiO$_2$/Si$_3$N$_4$ phased out around year 2005
  Growing reliability problems
  Unacceptable leakage
  SiO$_2$ interface layer tolerated till year 2014

- Solution?
  Design rules $\Rightarrow C_{ox} \Rightarrow$ (film thickness) $\sim$ (dielectric constant K)
  SiO$_2$ has K $\sim$4
  Gate dielectric with $20 < K < 40$ is optimal
  Leading candidates: TM and RE oxides (ionic compounds)

- Requirements:
  Thermal stability (must survive some secs at 900$^\circ$C)
  Good growth on Si(001); CVD strongly preferred
  No strange chemistry!
  Reasonably etchable, insoluble in water
  Band offsets sufficient to block leakage
  Interface state density comparable to SiO$_2$/Si(001)
HIGH-K MATERIALS AND AB INITIO CALCULATIONS

• Ab initio studies are expected to:
  Provide insight needed in design of deposition techniques
  Give early warning about reliability problems

• Several groups are active
  Motorola, Phoenix, AZ
  Stanford University, Stanford, CA
  IHP, Frankfurt(Oder), DE

• Example: Hf and Pr oxides on Si(001) surfaces (FHImd, [1])
  Bulk oxides: atomic and electronic structure
  Interfaces to Si(001) and bonding incompatibility

**TM and RE dioxides: fluorite structure**

*M* \(_2\) \(O_4\)

\((M^{+4})_2(O^{-2})_4\)

J. Dąbrowski, V. Zavodinsky, A. Fleszar, Microelectronics Reliability 7, 1093 (2001)
SUBSTRATE RECONSTRUCTION

Si(001) 3x1 substrate

Hf$^{4+}$(O$^{2-}$)$_2$
Pr$^{4+}$(O$^{2-}$)$_2$
BONDING INCOMPATIBILITY

Stoichiometric dioxide surface: ionic, no electrons to share

Si(001) 3x1 surface: covalent, many electrons to share
DIOXIDES: INTERFACE CHARGE TRANSFER

- Thumb rules for oxygen charge collected from metal atoms:
  - The charge is -2 when all O neighbors are metal
  - The charge tends to be -1 when one O neighbor is silicon

Fundamental structure of the interface
Each interface O collected 1 electron
Excess electrons forced into CB

Interface enriched in oxygen
Some interface O collected 2 electrons
Excess charge trapped
**Pr OXIDES: CUBIC STRUCTURES**

- **Cubic PrO$_2$** $(Pr_2O_4)$
  - $(Pr^{4+})_2(O^{2-})_4$

- **Cubic Pr$_2$O$_3$**
  - $(Pr^{3+})_2(O^{2-})_3$
SEQUIOXIDES: INTERFACE CHARGE TRANSFER

O vacancy at the interface filled
2 electrons in CB
Charge transfer from Pr to O: -4

Si dimer oxidized, O\textsubscript{v} in film filled
Energy gap
Charge transfer from Pr to O: -6
NITROGEN: INTERFACE DIPOLE CONTROL

**Oxygen at the interface**
Strong interface dipole

**Nitrogen at the interface**
Weak interface dipole

\[ \Delta E_{CB} \]
\[ \Delta V \]
\[ \Delta E_{VB} \]
**HEXAGONAL Pr$_2$O$_3$: WEAK DIPOLE MOMENT**

- Thumb rules for oxygen charge collected from metal atoms:
  - $O^{-2}$ when all neighbors are Pr
  - $O^{-1}$ when one neighbor is Si

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**Bulk dipoles and surface charge**

**Interfacial O can compensate charge loss**
XPS PEAKS REVEAL THE INTERFACE DIPOLE

- Two different phases observed in XRD:
  - Cubic (red lines)
  - Hexagonal (black lines)
- Core level peaks of Pr and O shift from hexagonal to cubic
  - Shift in the same direction
  - Shift by the same amount
  - The shift is consistent with the interface models
HIGH-K DIELECTRICS: SUMMARY

• Gate leakage increases exponentially with decreasing $t_{ox}$
  SiO$_2$ gate oxide phased out by the year 2005 (L=65nm) [1]
  SiO$_2$ interface layer tolerated till the year 2014 (L=35nm) [1]
  New gate dielectric will have high dielectric constant $K$ (30-40) [1]

• Industry DOES NOT KNOW what high-K material will be used
  Intensive materials science research is needed [1]
  - Dielectric properties of thin films? (K, reliability)
  - Electrical properties of interfaces? (charge traps, band offsets)
  - Interface SiO$_2$ layer formation?
  - Thermal stability?

• Example: Hf and Pr oxides on Si(001) substrates (FHImd, [2])
  Ionic/covalent interface $\Rightarrow$ stoichiometric interface is metallic
  Composition changes $\Rightarrow$ dipole changes $\Rightarrow$ band offsets changes
  Understanding the interface allows process control (in-situ XPS)

SUMMARY AND OUTLOOK

• Ab initio studies may contribute to CMOS miniaturization efforts
  Atomistic FEOL process simulator with ab initio input already works

• We considered three groups of examples:
  1. FEOL process simulation
     Charge granularity strongly affects MOSFET parameters (50 nm)
     FHImd example: Donor segregation to SiO$_2$/Si(001) interfaces
  2. Oxide reliability predictions
     Breakdown mechanism needed for reasonable predictions
     FHImd example: Microscopic sequence of breakdown process
  3. New material will soon replace SiO$_2$ as gate oxide
     Intensive materials science research is needed
     FHImd example: interfaces between Si(001) and Pr and Hf oxides

• 2000 IRTS on Modelling and Simulation Technology Requirements:
  2000: Model alternate dielectrics, gate oxide reliability
  2003: Interface interactions, extended defects, dislocations
  2003: Reliability of interconnects (stress, electromigration)
  2008: Mestastable activation, doping from solid sources
  2008: Ab initio simulation of deposited material properties
  2011: Computer engineered materials and process recipes
**CREDITS**

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<tr>
<th>Name</th>
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<td>IHP; MBE deposition of Pr oxides, XPS</td>
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<td>A. Fleszar</td>
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<td>V. Zavodinsky</td>
<td>IHP and IACP Vladivostok, Russia; ab initio</td>
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Calculations done on Cray T3E cluster in Jülich, project hfo06
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